High-speed Data Playback of the VLBI Hardware Correlator

Jiangying Gan, Zhijun Xu, Shaoguang Guo

Abstract VLBI (Very Long Baseline Interferometry) is an important radio astronomy technique and is widely used in deep-space probes and high-precision measurements. The performance of the correlator, as the core data pre-processing equipment of VLBI, is very important. At present, the Chinese VLBI data acquisition system (CDAS) can collect 2 Gbps of data, and a multi-band combination can reach 16/32 Gbps. To ensure that the requirements of high speed and high precision are met, Uniboard was used as the hardware platform, 10 G Ethernet was used as the data playback interface, and 1 G Ethernet was used as the control interface. Also research was done into the VLBI data playback, which reaches speeds up to 4 Gbps for a single CDAS, and a pre-processing method that provides data correction and data decoding specific to the VLBI data characteristics has been designed. Now we have finished the preliminary system, and here we will show the design and some results.

Keywords VLBI, Hardware Correlator, data playback, high-speed

1 Introduction

VLBI (Very Long Baseline Interferometry) is an important radio astronomy technique and is widely used in deep-space probes and in high-precision measurements. We have successfully used it to perform VLBI observations for several Chang'E missions [1]. Figure 1 is the Chinese VLBI Center architecture. The VLBI center is comprised of VLBI stations, data preprocessing, a correlator, a POST correlator, SKD, orbit determination, position determination, and so on. The hardware correlator is the VLBI core data preprocessing equipment, and it can calculate important parameters such as the delay, delay rate, correlation amplitude, interferometric phase, and so on.

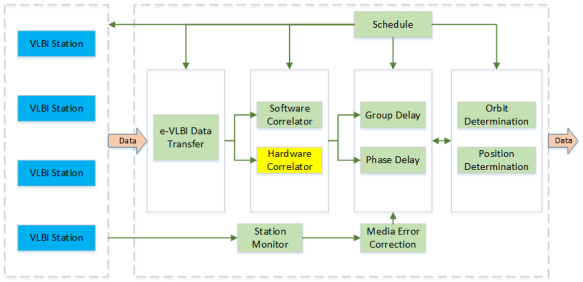

Fig. 1 Chinese VLBI Center.

Already in use, the hardware correlator has five FPGAs, which are configured in two columns. The front column contains four FPGAs to process data from four stations, and the back column contains one FPGA, which processes all channels of data from four stations at the same time. So the speed of the system is restricted. Now, our team has used a Uniboard as the hardware platform. The Uniboard, as the name suggests, is a universal processing platform which will be used in multiple processing applications such as the future EVN correlator. The board consists of eight processing FPGAs configured in two columns. The front column contains the front nodes. These FPGAs are each connected to four 10 GbE SFP+ inputs making copper and optical interfacing possible. Via mesh on the board, a front node is connected to each back node

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with a 10 Gbps link. The back side or back node FPGA is connected to a backplane. The control of the board is done via an onboard 1 GbE switch with four copper interfaces on the front panel and eight 1 GbE connections, one for each processing FPGA [2].

2 VLBI Data Playback System

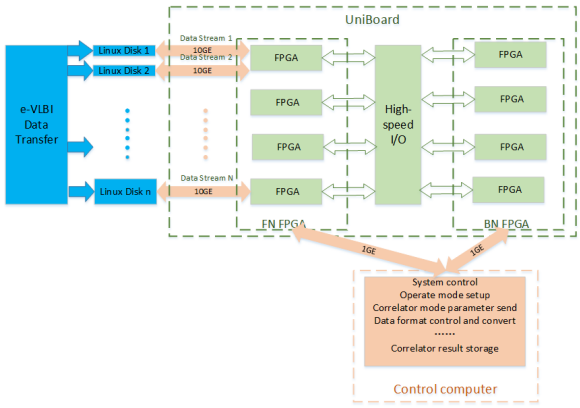

Fig. 2 Uniboard hardware correlator system.

In Figure 2 a block diagram of the Uniboard showing the connections can be seen [3]. The system has characteristics such as:

- Eight processing FPGAs are divided into four front FPGAs and four back FPGAs.
- One station can correspond to one 10 GbE interface, so each front FPGA can accomodate four stations at most.
- Four back FPGAs synchronously process all channels of data, so that data processing can occur more quickly.
- The 1 GbE connection can be used not only to control every board, but also to send the data resUlts to a control computer.

VLBI Data Playback includes a 10 GbE interface, a data playback control module, a data receiver and memory, a strip-head module, a cross switch, a fan-in, a SOPC system, and a 1GbE interface [4]. In Figure 3, the 1 marks the 10 Gb Ethernet interface initialization and control parameters, the 2 marks the playback parameters — including reset, start time, stop time, fan-in code, data bit, FFT size and so on, and the 3 indicates that frame header information is sent to a control computer in real-time to ensure time synchronization.

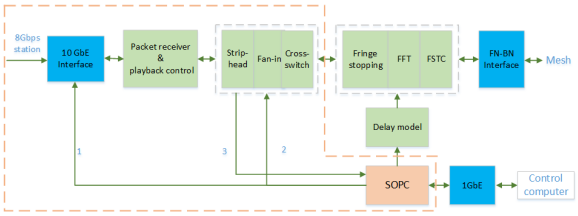

Fig. 3 One station front FPGA.

2.1 10GbE Module

The 10 GbE Network module includes a 10 GbE interface and a data playback control module, which is used to receive data, cache data, and control data playback. Figure 4 is the 10GbE communication and control block diagram. It uses an ACK to control the data playback start or stop. The processing is:

- A Linux disk sends N packets to the FPGA via 10 GbE and waits for a replay packet.
- The FPGA receives N packets and if the post-processing is not full, then sends a replay packet to the Linux disk.
- The Linux disk waits until it receives the ACK packet and then continues to send data packets.

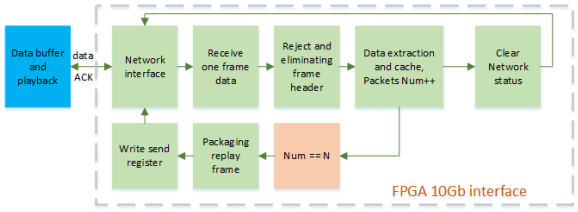

Fig. 4 FPGA 10 G interface.

In theory, the speed of data transmission is 10 G per second for the no load condition and could reach 8 Gbps for pre-processing, but it only reaches 4 Gbps in fact.

2.2 SOPC

The SOPC system is the bridge between the embedded software core system and the hardware IP module, intended to maintain data communication on both sides. The embedded software system NiosII's main functions are to:

- Receive and analyze the network packets and write data to the corresponding hardware IP module.
- Receive data from the hardware IP module and process and send information to the control computer.

The 1 GbE is used to receive data from the control computer and send the data to the target computer. The 1 GbE receives parameter packages for each processing FPGA and sends confirmation information. It also sends results to a PC when the TX data mode is triggered. The 1 GbE Ethernet transmission has two operating modes:

1. RX-TX mode. Receives the 1 GbE packets at first and sends replay packets afterwards.
2. TX only. Packages and sends data to the control computer under control.

Figure 5 shows the RX-TX mode working state.

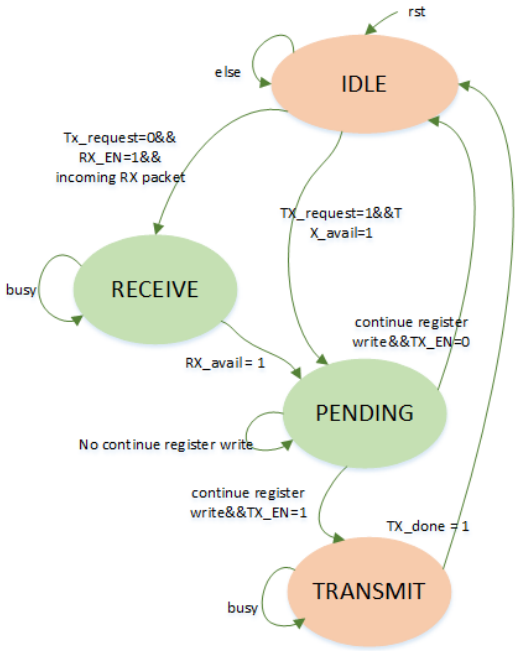

Fig. 5 1 GbE RX-TX mode.

3 Analysis

Figure 6 shows the results of real-time correlation of the data from the CE5-T1 (Chinese Lunar Mission). There are four stations, but the pictures only show two stations. Real-time correlation of the mission data gives the same results as are obtained from correlation using the current correlator.

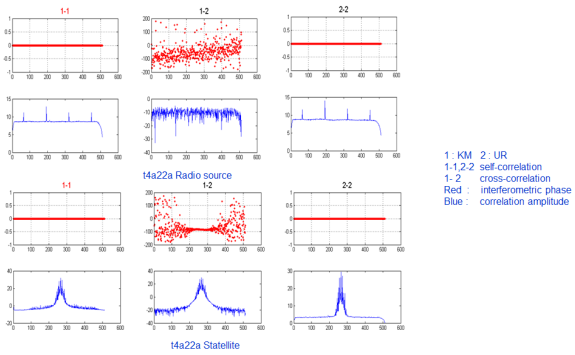

Fig. 6 Results of correlation.

4 Conclusions

The Uniboard correlator has already been finished, and some of its characteristics are shown in Table 1.

Table 1 Characteristics of the Uniboard correlator.

Mode	Near Real-time	Real-time
10 GbE Interface	4 Gbps	8 Gbps
IO Interface	6.25 Gbps	6.25 Gbps
Delay Tolerance	20 s	1 s
Buffering	Disk	Memory
Design Difficulty	10 GbE, high speed IO	DDR3, System
Applications	Deep space exploration	VGOS, SKA

But some capabilities need to be improved, and more astronomical applications will be added.

5 Future Plan

As a near-real-time-style correlator, the data latency needs to be fewer than 25 seconds during the CE-3 mis-

sion [5], and the number of stations must be fewer than five. So some work must still be done to meet more requirements for the new mission, such as: like:

- Support of 4, 8, and 16 bit sampled data,
- VDIF, VSR format data playback,
- Support of more stations (six/eight or more),
- Multi-target processing,
- Multi-bandwidth processing, and
- Adding DDR3 to cache data.

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